Internship Description

SoC Modules Formal Verification

(SM-STC 004 / 2024)

What we offer

Company	**SILICON MOBILITY SAS** *(registration number 815 085 659 000 RCS Grasse)* Head office : Les Aqueducs – Bât 2 – 535, route des Lucioles – 06560 Valbonne Sophia-Antipolis The Automotive industry is living a revolution. Electrification, autonomous driving, diverse mobility, and connectivity are trends that are changing the industry's rules. Among all decisive topics revolutionizing cars in the next future, Silicon Mobility is committed to supporting the rapid advent of electric and hybrid cars. Silicon Mobility is a technology leader for cleaner, safer, and smarter mobility. The company designs, develops and sells flexible, real-time, safe, and open semiconductor solutions for the automotive industry used to increase energy efficiency and reduce pollutant emissions while keeping passengers safe. We are looking for a motivated candidate to join our company in Sophia-Antipolis on the French Riviera. Please contact us: **internship2024@silicon-mobility.com**
Offer ref.	SM-STC 004-2024
Subject – Offer title	SoC Modules Formal Verification
Duration	5-6 months– between February/March/April and September 2024
Work hours	35 hours per week, job location at Silicon Mobility office
Education	Last year of Masters (BAC+5 or equivalent)
Content/ mission	As part of its product roadmap, Silicon-Mobility is developing its new generation of System-on-Chip called OLEA® FPCU (Filed Programmable Control Unit). This innovative architectural component is based on a multi-core architecture combined with a patented real-time subsystem including an embedded programmable logic structure. The proposed internship addresses a specific need of the IP development team: the formal verification of critical modules. The formal verification will allow the design team to accelerate the verification (finding bugs early in the development flow) and gain confidence in the quality of the RTL code on some critical functionalities. The following activities will be carried out during the internship: • Set up a flow to be able to run Formal Proof Verification (FPV) on SystemVerilog assertion using Cadence/Siemens or Synopsys tool (tool choice to be discussed). • Define system Verilog assertions to check some critical features on one or several critical IPs. • Debug the module (with the designer) if errors are found. • Evaluate the benefit of formal proof verification.
Profile required	For this internship, we are looking for a student in the field of microelectronics. A strong general culture in SoC development (front end) is required (RTL design, Verification...) Knowledge of the Verilog or VHDL language. Some knowledge of Formal Verification is a plus. The qualities of autonomy, rigor, and ability to work as a team are important. A good level of English is required.
Expected Skills/knowledge	• Knowledge development on Systems on Chip (SoC) • Digital module development and verification in Verilog or VHDL • Use of simulation and digital debug tools (QuestaSim or equivalent) • English
Remuneration	€1400/month + Tickets Restaurant + Public transport