Internship Description

Design for Testability of SoC and Hard Macro

(SM- STC002 / 2024)

What we offer

Company	**SILICON MOBILITY SAS** *(registration number 815 085 659 000 RCS Grasse)* Head office : Les Aqueducs – Bât 2 – 535, route des Lucioles – 06560 Valbonne Sophia-Antipolis The Automotive industry is living a revolution. Electrification, autonomous driving, diverse mobility, and connectivity are trends that are changing the industry's rules. Among all decisive topics revolutionizing cars in the next future, Silicon Mobility is committed to supporting the rapid advent of electric and hybrid cars. Silicon Mobility is a technology leader for cleaner, safer, and smarter mobility. The company designs, develops and sells flexible, real-time, safe, and open semiconductor solutions for the automotive industry used to increase energy efficiency and reduce pollutant emissions while keeping passengers safe. We are looking for a motivated candidate to join our company in Sophia-Antipolis on the French Riviera. Please contact us: **internship2024@silicon-mobility.com**
Offer ref.	SM-STC 002-2024
Subject – Offer title	Design For Testability of SoC and Hard Macro
Duration	5-6 months– between February/March/April and September 2024
Work hours	35 hours per week, job location at Silicon Mobility office
Education	Last year of Masters (BAC+5 or equivalent)
Content/ mission	As member of the System on Chip (SoC) Design for Test (DFT) team, you will have the opportunity to participate in the development of the testability flow from RTL to Manufacturing. You will be involved in the implementation and the validation of the DFT features at Hard-macro and SoC level. Since Silicon Mobility develops chips for automotive applications, you will be exposed to functional safety methodologies and technics responding to ISO 26262 requirements. Being in the middle-end of the development process, the interactions between the RTL and the backend team are a key point. You will be responsible for: • DataSheet, Userguide and Testguide documents understanding. • DFT implementation and testing of Analog/Mixed-signal IP. • Scan implementation and validation at Hard-macro level. • MemoryBist implementation and validation at Hard-macro level. • Boundary scan implementation at SoC level.
Profile required	• Good communication skills. • Effective technical English. • Autonomous at work • Good team spirit • Proactive
Expected Skills/knowledge	• Knowledge of RTL coding (Verilog, System Verilog) • Knowledge of scripting (TCL, Perl, Makefile, csh, bash) • First academic EDA tools experience. • Academic experience in JTAG, IJTAG is a plus. • Theoretical knowledge in boundary scan test • Theoretical knowledge in LogicBist test • Theoretical knowledge in Memory Built-In Self-Test • Knowledge of simulation tools • Knowledge of Automatic Test Patterns Generator • Theoretical knowledge of Scan structure, hierarchical test flow is a plus
Remuneration	€1400/month + Tickets Restaurant + Public transport