Internship Description

SoC Physical Design

(SM-STC002 / 2023)

What we offer

Company	**SILICON MOBILITY SAS** *(immatriculée 815 085 659 000 28 RCS Grasse)* Siege social : Les Aqueducs – Bât 2 – 535, route des Lucioles – 06560 Valbonne Sophia-Antipolis The Automotive industry is living a revolution. Electrification, autonomous driving, diverse mobility, connectivity are trends that are drastically changing the industry's rules. Among all decisive topics revolutionizing cars in the next future, Silicon Mobility is committed to support the rapid advent of electric and hybrid cars. Silicon Mobility is a technology leader for cleaner, safer and smarter mobility. The company designs, develops and sells flexible, real-time, safe and open semiconductor solutions for the automotive industry used to increase energy efficiency and reduce pollutant emissions while keeping passengers safe. We are looking for a good candidate to join our R&D team working in Sophia-Antipolis on the Côte d'Azur. Please contact us: **internship2023@silicon-mobility.com**
Offer ref.	SM-STC002-2023
Subject – Offer title	SoC Physical Design
Duration	6 months – between February/March/April and September 2023
Work hours	35 hours a week at silicon Mobility office
Education	Last year of Masters (BAC+5 or equivalent)
Content / mission	As part of its product roadmap, Silicon-Mobility is developing its new generation of FPCU System-on-Chip. This innovative architectural component is based on a multi-core architecture combined with a patented real-time subsystem including an embedded programmable logic structure. As part of the Physical Design team, you will have the opportunity to evaluate new tools, develop and integrate new design techniques in our flow before applying them at block or SoC level on the current project. You will explore the technology process and will be trained to functional safety methodologies and technics for the automotive market (ISO 26262). On a sub-block, you will contribute to all the aspects of the Physical Design from RTL to GDSII using the leading EDA tools of the industry. You will be responsible for: • Assessing, integrating new tools and physical design techniques through scripts. Then applying at SoC or block level respecting design and technology constraints. • Identifying issues with IPs, process technology, and/or EDA tools. • Performing physical design from RTL to GDS, including DRC, LVS. • Analyzing, interpreting, and presenting implementation results.
Profile required	• Curious and keen to learn. • Collaborative and agile. • Good debugging and analytical skills. • Able to work independently under local project lead/mentorship. • Knowledge of logic synthesis, place and route concepts. • Scripting skills in any programming language (TCL, Makefile, Shell, Python, Perl…) is a plus. • Experience of layout of ICs with analog content is a bonus. • An understanding of semiconductor fabrication technology. • Good verbal and written communication skills.

Expected skills / knowledge	• Custom Compiler and Fusion for analog & digital co-designing. • Custom Analog routing in highly constrained and complex SoC level. • Understand a complete RTL2GDSII flow. • Understand specific design/technology technics. • Knowledge of semiconductor foundry process for automotive. • Usage of configuration management tools (SVN), Load sharing (LSF), Makefile, Tcl… • Knowledge of Systems on Chip (SoC) development program and team's relationships.
Remuneration	1400€/month + Tickets Restaurant