Internship Description

IP Verification with SystemVerilog (SM-STC002 / 2022)

What we offer

Company	**SILICON MOBILITY SAS** *(registration number 815 085 659 000 RCS Grasse)* Head office : Les Aqueducs – Bât 2 – 535, route des Lucioles – 06560 Valbonne Sophia-Antipolis The Automotive industry is living a revolution. Electrification, autonomous driving, diverse mobility, and connectivity are trends that are changing the industry's rules. Among all decisive topics revolutionizing cars in the next future, Silicon Mobility is committed to supporting the rapid advent of electric and hybrid cars. Silicon Mobility is a technology leader for cleaner, safer, and smarter mobility. The company designs, develops and sells flexible, real-time, safe, and open semiconductor solutions for the automotive industry used to increase energy efficiency and reduce pollutant emissions while keeping passengers safe. We are looking for a motivated candidate to join our company in Sophia-Antipolis on the French Riviera. Please contact us: **internship2022@silicon-mobility.com**
Offer ref.	SM-STC002-2022
Subject – Offer title	IP Verification with SystemVerilog
Duration	6 months – between February/March/April and September 2022
Work hours	35 hours a week at Silicon Mobility office
Education	Last year of Masters degree in Electronics Engineering / Microelectronics (BAC+5 or equivalent)
Content/ mission	Silicon Mobility is developing a System on Chip named OLEA® FPCU. Each FPCU includes several modules (IP). To guarantee the IP does not contain bug, it is necessary to make intensive verification. To do this verification Silicon put in place a method based on SystemVerilog language and Universal Verification Methodology (UVM). The objective of the internship is to put in place this verification method on a new IP module. The intern will be part of the FPCU Front-End team. This project will be divided in 3 main phases: 1. Exploration/Definition, the intern will have to acquire knowledge of: a. IP Module to verify b. SystemVerilog language and Verification method c. Write the verification test plan of the IP module 2. Development, the intern will: a. Define and write the structure of the verification b. Write the different test scenarios c. Set up mechanisms to measure coverage 3. Verification debug, in this phase the intern will: a. Run simulation under QuestaSim environment b. Debug the verification tests c. Check the requirements tracability
Profile required	For this internship, we are looking for a candidate with: • knowledge of Hardware design for System On Chip (Verilog or VHDL language) • Knowledge of an Object Oriented Language (Java or C++) • knowledge of SystemVerilog and UVM methodology (would be appreciated) • good English level • autonomy, rigor, strong team spirit, strong problem-solving skills

Expected Skills/knowledge	• IP verification methodology • UVM methodology • SystemVerilog language • General knowledge in System On Chip development • Quality approach
Remuneration	€1000/month + Tickets Restaurant + Public transportation