Apprenticeship Description

IP Verification with System Verilog

(SM-STA001 / 2022)

Internship Description

Company	**SILICON MOBILITY SAS** *(numbered 815 085 659 000 28 RCS Grasse)* Head office : Les Aqueducs – Bât 2 – 535, route des Lucioles – 06560 Valbonne Sophia-Antipolis The Automotive industry is living a revolution. Electrification, autonomous driving, diverse mobility, connectivity are trends that are drastically changing the industry's rules. Among all decisive topics revolutionizing cars in the next future, Silicon Mobility is committed to supporting the rapid advent of electric and hybrid cars. Silicon Mobility is a technology leader for cleaner, safer and smarter mobility. The company designs, develops and sells flexible, real-time, safe and open semiconductor solutions for the automotive industry used to increase energy efficiency and reduce pollutant emissions while keeping passengers safe. We are looking for a good candidate to join our R&D team working in Sophia-Antipolis on the French Riviera. Please contact us: **internship2022@silicon-mobility.com**
Offer Number	SM-STA001-2022
Project Title	IP Verification with System Verilog
Period	12 months– between September 2022 and September 2023
Working hours	35 hours a week at Silicon Mobility office
Income	From 1300€/month + Tickets Restaurant
Student level	Last year of Masters (BAC+5 or equivalent)

Project Description	Silicon Mobility is developing System on Chip with an FPCU architecture. Each chip includes several hardware modules (IP). To guarantee that the IP is bug-free, it is necessary to make intensive verifications. Silicon Mobility is using a verification method based on SystemVerilog language and Universal Verification Methodology (UVM). The objective of the internship is to put in place this verification method on a newly developed IP module. The intern will be part of the FPCU Front-End design team.
	
	This project will be divided into 3 main phases:
	• Exploration/Definition, the intern will have to acquire knowledge of:
	  ○ IP module to verify
	  ○ SystemVerilog language and verification method
	  ○ Write the verification test plan of the IP module
	• Development, the intern will:
	  ○ Define and write the structure of the verification
	  ○ Write the different test scenarios
	  ○ Set up mechanisms to measure coverage
	• Verification debug, in this phase the intern will:
	  ○ Run simulation under QuestaSim environment
	  ○ Debug the verification tests
	  ○ Check the requirements for tracability

Profile	For this internship, we are looking for a candidate with: • knowledge of Hardware design for System On Chip (Verilog or VHDL language) • Knowledge of an Object-Oriented Language (Java or C++) • knowledge of SystemVerilog and UVM methodology (would be appreciated) • good English level • autonomy, rigor, strong team spirit, strong problem-solving skills
Skills developed	• IP verification methodology • UVM methodology • SystemVerilog language • General knowledge in System On Chip development • Quality approach