Silicon Mobility
535 Route des Lucioles
Les Aqueducs – Bâtiment 2
06560 Valbonne /
Sophia Antipolis France

Location: Sophia-Antipolis, France
Employment type: Experienced Professional
Contract type: Permanent position

Ref: RD_DFT_MNGR

DFT ARCHITECT MANAGER

The Automotive industry is living a revolution. Electrification, autonomous driving, diverse mobility, connectivity are trends that are drastically changing the industry's rules. Among all decisive topics revolutionizing cars in the next future, Silicon Mobility is committed to support the rapid advent of electric and hybrid cars.

Silicon Mobility is a technology leader for cleaner, safer and smarter mobility. The company designs, develops and sells flexible, real-time, safe and open semiconductor solutions for the automotive industry used to increase energy efficiency and reduce pollutant emissions while keeping passengers safe.

The Company is opening a "DFT Architect Manager" position in its main Research and Development center ideally located in the Sophia-Antipolis Technology Park on the French Riviera.

You are a brilliant and passionate by Design For Test for System on Chip ? You want to support the development of disruptive products accelerating the car's powertrain electrification? At Silicon Mobility, we like to light up our employee's potential. Are you up for the challenge? **Contact** us**:** send your resume and cover letter to hr@silicon-mobility.com

ROLE & MISSIONS

DFT Architect Manager is part of the engineering team and participates in the SoC design of Silicon Mobility. The main responsibilities are:

- DFT strategy and methodology for all SoC development.
- DFT architecture of SoC for all the features (Memories, logic, IOs, analog cells…..);
- Definition and redaction of DFT specifications;
- Definition and development of DFT hardware verification plan
- Management of a team of DFT engineers (internal or external) :
    - Participate in team staff recruitment (internal or external)
    - Define the tasks
    - Follow the tasks and objectives
- DFT tasks expert :
    - Review of IPs and SOC architecture for compliance with DFT objectives
    - RTL coding or generation (memory BIST generation, boundary scan insertion, logic BIST, test manager, …);
    - DFT top level integration
    - Scan insertion and coverage review;
    - Static timing analysis (STA);
    - Generation of test pattern;
    - RTL and GLS simulation of test pattern;
- Management of DFT tools (main interface with EDA provider for DFT tools)
- Development of DFT design flow automation scripts
- Main interface with Test-House for debug on tester to put in place production tests;
- DFT Technology watch : methodology and tools

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REQUIRED SKILLS AND EXPERIENCE

EDUCATION:

- Engineering degree in microelectronics

TECHNICAL SKILLS & EXPERIENCE:

- A minimum of 5 years of experience in DFT architecture definition and DFT implementation.
- Good knowledge in RTL Verilog or VHDL, STIL language, simulation tools (Modelsim/VCS or others), scan insertion tools (Synopsys DC, DFT Compiler), STA tools (Synopsys Primetime) and DFT tools (Synopsys SMS/SHS, DC LBIST, Tetramax, Tessent MBIST/LBIST).
- Good knowledge in scripting languages (Shell, Makefile, Perl, …)
- Good working knowledge of various protocol (JTAG, IEEE1500)
- Experience in team management and/or task subcontracting.
- Knowledge on production test program for production tester

LANGUAGE SKILLS:

- Fluent in English

BEHAVIORAL SKILLS:

- Be self-motivated, pro-active, flexible and capable of accepting new challenges.
- Demonstrate strong communication skills at technical and management levels.
- Be able to work well across different teams within Silicon Mobility to understand their individual needs and constraints.